CLAIMS

What is claimed is:

1. An apparatus for detecting an event, comprising:

a bistable memory device, said bistable memory device having an input adapted for detecting the occurrence of an event and an output representing a logic state of said bistable memory device, wherein said logic state is at either a first or a second logic level such that the logic level of said logic state changes each time the event is detected; and

a digital processor, said digital processor having an input coupled to the output of said bistable memory device, whereby said digital processor periodically reads said logic state and stores the logic level thereof, wherein said digital processor compares the logic level of a subsequently read logic state with the stored logic level so as to determine whether the stored logic level is the same or different than the logic level of said subsequently read logic state, if different then an event has occurred and if the same then no event has occurred.

2. The apparatus of claim 1, wherein said bistable memory device is a flip-flop.

3. The apparatus of claim 2, wherein said flip-flop is selected from the group consisting of D, J-K, R-S and toggle flip-flops.

4. The apparatus of claim 1, wherein said bistable memory device is a counter.

5. The apparatus of claim 4, wherein said counter is selected from the group consisting of an asynchronous and a synchronous counter.

6. The apparatus of claim 1, wherein said bistable memory device is a latch.

7. The apparatus of claim 1, wherein said digital processor is selected from the group consisting of a microcontroller, a microprocessor, a programmable logic array and an application specific integrated circuit.

8. The apparatus of claim 1, wherein said digital processor comprises a central processing unit, a random access memory and a read only memory.

9. The apparatus of claim 1, wherein said digital processor comprises a bistable memory device and logic gates.

10. The apparatus of claim 9, wherein said logic gates are selected from the group consisting of inverter, OR, NOR, AND, NAND, XOR and XNOR.

11. The apparatus of claim 1, further comprising a plurality of bistable memory devices for detecting a plurality of events, wherein said plurality of bistable memory devices are coupled to said digital processor.

12. A method for detecting an event with a bistable memory device and a digital processor, said method comprising the steps of:

changing a logic state of a bistable memory device each time an event is detected, wherein the logic state is at either a first or a second logic level;

reading the logic state of the bistable memory device with a digital processor;

storing the logic level of the read logic state in the digital processor; and

comparing the stored logic level with the logic level of a subsequently read logic state so as to determine whether the stored logic level is the same or different than the logic level of said subsequently read logic state, if different then an event has occurred and if the same then no event has occurred.

13. The method of claim 12, wherein said bistable memory device is a flip-flop.

14. The method of claim 13, wherein said flip-flop is selected from the group consisting of D, J-K, R-S and toggle flip-flops.

15. The method of claim 12, wherein said bistable memory device is a counter.

16. The method of claim 15, wherein said counter is selected from the group consisting of an asynchronous and a synchronous counter.

17. The method of claim 12, wherein said bistable memory device is a latch.

18. The method of claim 12, wherein said digital processor is selected from the group consisting of a microcontroller, a microprocessor, a programmable logic array and an application specific integrated circuit.

19. The method of claim 12, wherein said digital processor comprises a central processing unit, a random access memory and a read only memory.

20. The method of claim 12, wherein said digital processor comprises a bistable memory device and logic gates.

21. The method of claim 12, further comprising the steps of:

providing a plurality of bistable memory devices for detecting a plurality of events;

changing a logic state of each of the plurality of bistable memory devices when a respective one of the plurality of events is detected, wherein the logic state is at either a first or a second logic level;

reading the logic state of each of the plurality of bistable memory devices with the digital processor;

storing the logic levels of each of the read logic states in the digital processor; and

comparing each of the stored logic levels with the logic levels of subsequently read logic states so as to determine whether each of the stored logic levels is the same or different than the logic levels of the respective ones of said

22. The method of claim 12, where the first logic level is a logic low and the second logic level is a logic high.

23. The method of claim 12, where the first logic level is a logic high and the second logic level is a logic low.

24. The apparatus of claim 1, further comprising a logic circuit for producing a clock pulse each time a transition from a low to a high or a high to a low logic level is detected.

25. The apparatus of claim 24, wherein said logic circuit is connected between the event and the input of said bistable memory device.

26. The apparatus of claim 25, wherein said logic circuit comprises an XOR and an even number of inverters.

27. A digital system adapted for serial digital data communications, said system comprising:

a transmitter and a receiver, said transmitter being adapted for sending serially encoded digital information and said receiver being adapted for receiving serially encoded digital information;

a computer adapted for serial digital data communications;

an event detector comprising:

a first bistable memory device, said bistable memory device having an input adapted for detecting the occurrence of an event and an output

representing a logic state of said bistable memory device, wherein said logic state is at either a first or a second logic level such that the logic level of said logic state changes each time the event is detected;

a second bistable memory device, said bistable memory device having an input adapted for detecting the occurrence of an event and an output representing a logic state of said bistable memory device, wherein said logic state is at either a first or a second logic level such that the logic level of said logic state changes each time the event is detected; and

a digital processor, said digital processor having an input coupled to the output of said first bistable memory device and another input coupled to the output of said second bistable memory device, whereby said digital processor periodically reads said logic states and stores the logic levels thereof, wherein said digital processor compares the logic level of a subsequently read logic state with the stored logic level so as to determine whether the stored logic level is the same or different than the logic level of said subsequently read logic state, if different then an event has occurred and if the same then no event has occurred;

wherein said event detector is coupled between said transmitter said computer, and said receiver and said computer such that said first bistable memory device is coupled to said receiver and said second bistable memory device is coupled to a serial output of said computer.

28. The digital system of claim 27, wherein the transmission of said transmitter is selected from the group consisting of infrared, ultraviolet, radio frequency, microwave and ultrasonic.

29. The digital system of claim 27, wherein the reception of said receiver is selected from the group consisting of infrared, ultraviolet, radio frequency, microwave and ultrasonic.

30. The digital system of claim 27, wherein said computer is selected from the group consisting of a microcontroller, microprocessor, digital signal processor, reduced instruction set computer (RISC), complex instruction set computer (CISC).